

Claims

1. A package cover having a cavity for receiving an infrared detector and a window area for transmitting infrared radiation to the detector, an interior surface of the window area within the cavity having a field of posts shaped and spaced so as to form an antireflection element for infrared radiation transmitted through the window area.
2. The cover of claim 1 where the posts are upstanding from a ground level below the bottom surface of the cavity.
3. The cover of claim 2 where the tops of the posts are flush with the bottom surface of the cavity.
4. The cover of claim 1 where the posts are holes depressed below the bottom surface of the cavity.
5. The cover of claim 1 where the cover is a silicon wafer.
6. The cover of claim 5 where the cavity is about 0-500 μ m deep.
7. The cover of claim 6 where the cavity is about 10-100 μ m deep.
8. The cover of claim 5 where the cavity is surrounded by a perimeter area.
9. The cover of claim 1 where the posts form a pattern having two orthogonal directions of symmetry.
10. The cover of claim 1 where the posts are square.

11. The cover of claim 1 where the posts are right circular cylinders.
12. The cover of claim 11 where the posts have a diameter in the approximate range of $1\mu\text{m}$ to $10\mu\text{m}$.
13. The cover of claim 12 where the posts have a spacing less than about $6\mu\text{m}$.
14. The cover of claim 1 where the posts have non-vertical sidewalls.
15. The cover of claim 14 where the posts are substantially pyramidal.
16. The cover of claim 14 where the posts are substantially conical.
17. The cover of claim 1 where the posts are between about $0.2\mu\text{m}$ and about $4\mu\text{m}$ high.
18. The cover of claim 1 where the posts are equally spaced rows and columns.
19. The cover of claim 18 where the rows and columns are spaced less than about $6\mu\text{m}$ apart.
20. The cover of claim 1 where an exterior surface of the cover has an antireflective coating in the window area.
21. The cover of claim 20 where the antireflective layer comprises a further field of posts shaped and spaced so as to form an antireflection element.

22. An infrared detector, comprising:
an array of pixels for producing an electrical signal in response to incident infrared radiation;
a substrate for holding the array;
a package cover having a window in a cavity for transmitting the radiation to the array;
a field of spaced posts for reducing reflections of the infrared radiation in the window.
23. The detector of claim 22 further comprising a seal for joining a perimeter area of the cover to the substrate.
24. The detector of claim 23 where the cavity is evacuated.
25. The detector of claim 22 where the tops of the posts are substantially flush with a surface of the cavity.
26. The detector of claim 22 where the bottoms of the posts lie below the level of a surface of the cavity.
27. The detector of claim 22 where the array of pixels is a rectangular array of bolometers.
28. The detector of claim 22 further comprising detection circuits for processing an image signal from the detector.
29. The detector of claim 28 further comprising scanning circuits coupled to the detector.

30. The detector of claim 28 further comprising a display coupled to the detection circuits.
31. The detector of claim 30 further comprising scanning circuits coupled to both the detector and the display.
32. A method for fabricating an infrared optical element from a wafer of material capable of transmitting infrared radiation therethrough, comprising, in the order listed:
masking a surface of the wafer with a pattern defining a cross section of a field of posts;
etching the wafer surface so as to form the field of posts to a desired depth;
masking the field of posts with a shape defining a cavity in the surface of the wafer;
etching the wafer surface including the field of posts so as to form a cavity in the wafer.
33. The method of claim 32 where the second etching operation is performed such that the tops of the posts lie below the surface of the cavity.
34. The method of claim 32 where the second etching operation is performed such that tops of the posts are approximately flush with a bottom surface of the cavity.
35. The method of claim 32 where the second etching operation is performed such that bottoms of the posts lie below a bottom surface of the cavity.
36. The method of claim 32 where the cross section of the posts varies along their height.
37. The method of claim 36 where the cross section decreases along the height.

38. The method of claim 32 where the first etching operation is a reactive ion etch.
39. The method of claim 38 where the second etching operation is a reactive ion etch.
40. The method of claim 32 where the height of the posts after the second etching operation is in the approximate range of 0.5 μ m to 4 μ m.
41. The method of claim 32 further comprising applying an antireflection layer to a side of the wafer opposite the cavity.
42. The method of claim 32 further comprising mounting an infrared detector to the wafer so as to receive incident infrared radiation through the wafer.
43. The method of claim 42 where the infrared detector is an array of bolometer pixels.
44. The method of claim 42 further comprising mounting the detector to the wafer.
45. The method of claim 44 wherein the detector is hermetically sealed to the wafer.
46. The method of claim 44 further comprising evacuating the cavity.
47. A method for fabricating an infrared optical device, comprising:
masking a surface of a wafer of material capable of transmitting infrared radiation therethrough with a pattern defining a field of posts;
etching the wafer surface so as to form the field of posts to a desired height;
applying an antireflection element to the other surface of the wafer;
sealing the wafer to a substrate containing an array of bolometers.

48. The method of claim 47 further comprising evacuating a space between the wafer and the substrate.

49. The method of claim 47 where the posts have varying cross section along their height.

50. The method of claim 47 further comprising:
performing the above operations for a plurality of infrared optical devices on the same wafer;
dicing the wafer after sealing it to the substrate containing multiple arrays of bolometers;
thereafter, dicing the wafer and the substrate to separate individual ones of the devices.